This listing of claims will replace all prior versions and listings of the claims in this application:

Claims 1-4 (cancelled)

Claim 5 (currently amended) A synthesizer ~~of claim 4~~ comprising:

a phase lock loop circuit;

a microcontroller, coupled to and configured for optimizing a bandwidth characteristic of said phase lock loop over a range of variable output frequencies;

said microcontroller further configured for carrying out a self-calibration procedure for said phase lock loop;

said self-calibration procedure involving a monitoring of a tune voltage for a voltage-controlled oscillator and manipulation of inputs into said phase lock loop circuit;

wherein said inputs include a variable loop division ratio;

an integrator within said phase lock loop circuit;

wherein said microcontroller computes an integrator gain for said integrator and a tune sensitivity characteristic for said voltage controlled oscillator;

wherein said integrator further comprises an integrator op-amp, an integrator resistor and an integrator capacitor; and

further comprising a multiplexer for providing variable resistance paths into a first input of said op-amp, where said multiplexer is controlled by said microcontroller.

Claim 6 (original) A synthesizer of claim 5 further comprising a digital potentiometer which provides a signal to a second input to said op-amp.

Claim 7 (original) A synthesizer of claim 6 where said microcontroller further comprises an analog-to-digital converter for converting said analog tune voltage to a digital value.

Claim 8 (original) A synthesizer of claim 7 further comprising a modulation source configured to provide a signal to said digital potentiometer.

Claim 9 (original) A synthesizer of claim 8 wherein said microcontroller is a field programmable gate array.

Claim 10 (original) A synthesizer of claim 9 further comprising a phase detector having a gain of Kp, a loop division ratio of N, an integrator gain of M, a tune sensitivity characteristic of Kv, such that the bandwidth (BW) of the phase lock loop circuit is defined by BW = M x Kp x Kv/N.

Claim 11 (original) A synthesizer of claim 5 wherein a phase detector gain is controlled by the microcontroller.

Claims 12-14 (cancelled)

Claim 15 (currently amended) A synthesizer ~~of claim 14~~ comprising:

a phase lock loop circuit;

means for optimizing a bandwidth characteristic of said phase lock loop circuit over a range of variable output frequencies, and for carrying out a self-calibration procedure for said phase lock loop;

where said self-calibration procedure involves a monitoring of a tune voltage for a voltage-controlled oscillator and manipulation of inputs into said phase lock loop circuit;

an integrator within said phase lock loop circuit;

wherein said means for optimizing further computes an integrator gain for said integrator and a tune sensitivity characteristic for said voltage controlled oscillator;

wherein said integrator further comprises an integrator op-amp, an integrator resistor and an integrator capacitor; and

further comprising means for providing variable resistance paths into a first input of said op-amp;

where said variable resistance paths are controlled by said means for optimizing.

Claim 16 (original) A synthesizer of claim 15 further comprising a digital potentiometer which provides a signal to a second input to said op-amp.

Claim 17 (original) A synthesizer of claim 16 where said means for optimizing further is for converting said analog tune voltage to a digital value.

Claim 18 (original) A synthesizer of claim 17 further comprising means for providing a modulated signal to said digital potentiometer.

Claim 19 (original) A synthesizer of claim 15 further comprising a phase detector having a gain of Kp, a loop division ratio of N, an integrator gain of M, a tune sensitivity characteristic of Kv, such that the bandwidth (BW) of the phase lock loop circuit is defined by BW = M x Kp x Kv/N; and,

a phase detector gain is controlled by said means for optimizing.

Claim 20 (original) A method of calibrating a synthesizer with a phase lock loop circuit comprising the steps of:

providing a variable resistance path to an input of an integrator where said variable resistance is provided by a microcontroller manipulated multiplexer;

providing a tune voltage output signal from said integrator which is input into a voltage controlled oscillator;

monitoring said tune voltage output signal by a microcontroller; and

calibrating said phase lock by manipulating a loop division ratio and said variable resistance path and calculating a gain of said integrator and a tune sensitivity characteristic of said voltage-controlled oscillator across an operating range of said voltage-controlled oscillator.